RR1X2 Digital Latch Sensor Series

PRODUCT Pre-QUALIFICATION REPORT

August 15, 2019

Summary

This report documents the qualification and test results for Coto Technology's RR1X2 series of Sensor products.

The digital latch sensors are fabricated using Coto Technology's next generation TMR process and assembled in industry standard packages such as SOT23.

All of the environmental tests were performed at an accredited independent testing lab.

In total, 1,030 devices were tested with a variety of qualification stress tests under various test conditions. There were zero failures. Full qualification is in progress.

Reference Documents

JESD47I:	Stress-Test-Driven Qualification of Integrated Circuits
JESD22-A113:	Preconditioning MLS1
JESD22-A103:	High Temperature Storage Life (HTSL)
JESD22-A104:	Temperature Cycling
JESD22-A108:	Temperature, Bias, and Operating Life (HTOL)
JESD22-A118:	Unbiased HAST
JESD22-A110:	Biased HAST
JEDEC-JS001-2014:	ESD
JESD78:	Latch Up

Table of Contents

1. Product Tested /4
2. Definition of Qualification /4
3. Qualification Test Plan /5
4. Sampling Plan /6
5. Failure Criteria /6
6. Summary of Qualification Test Results /6
7. Conclusion /11
8. Revision History /12

1. Product Tested

The TMR Latch sensor products are fabricated using Coto Technology's next generation TMR process and assembled in industry standard packages.

All tests are performed by an accredited independent testing lab.

In total, 1,030 devices were stressed with a variety of qualification tests under various test conditions. Of the devices tested, there were zero failures during qualification testing.

2. Definition of Qualification

The RR1X2 series of products are defined as products meeting all of the following criteria:

- A single TMR process technology (TMR = magnetic field sensor process)
- The same design rules and process technology.

3. Qualification Test Plan

The product qualification test plan is outlined in Table 1. This plan is based on the guidelines of the JESD47I, *Stress-Test-Driven Qualification of Integrated Circuits*, published by JEDEC Solid State Technology Association.

Table 1 – List of Qualification Test

Test	Stress	Duration	Sample Size
Parametric Tests	Evaluate Data Sheet Spec. @ +25°C	N/A	All Devices Used for Qualification
Pre-Conditioning	Thermal, Mechanical for Package Integrity: • SOT23	MSL1	2 lots (520 units)
Temperature Cycling	Thermal Mechanical	-55°C and +125°C @ 3 cycles/hr, 1,000 cycles	2 lots (154 units)
Unbiased HAST	Thermal Moisture	+130°C, RH 85%, 96 hours	2 lots (154 units)
Biased HAST	Bias, Thermal Moisture	V_{DD} = 4.0 V @ +130°C, RH 85%, 96 hours	2 lots (154 units)
HTOL	Bias, Thermal	1,000 hours (See Bias Conditions in Table 5 of Section 6.5)	2 lots (154 units)
High Temperature Storage	Thermal, Material Relaxation	1,000 hours (See Static Bake Conditions in Table 6 of Section 6.6)	2 lots (154 units)
Latch-Up	Electrical	JESD78 (±200 mA)	1 lot
ESD	Human Body Model	JEDEC-JS001-2014	1 lot

HAST – Highly accelerated temperature/humidity stress test
HTOL – High temperature operation life

4. Sampling Plan

Random samples were selected for product qualification as shown in Table 1. Sample size meets or exceeds the number of samples recommended by JESD47I standard. Seventy-seven (77) sample units per lot were used for each stress test with 5% LTPD.

5. Failure Criteria

A device failure is defined as a condition in which a stressed device can no longer meet its datasheet specifications or it has consequential physical damage attributed to an environmental test.

6. Summary of Qualification Test Results

A summary of qualification test results is provided in following sections.

6.1. Pre-Conditioning

A total of 1,030 devices were pre-conditioned using JESD22-A113 level 1 procedures. Preconditioning is performed on samples before they are subjected to package-related stress tests. The samples were exposed to thermally stressful conditions equivalent to thermal conditions experienced by units during board soldering.

Table 1.2 – *Preconditioning* Results

Wafer Lot	MSL Level	Sample Size	Devices Failed	Test Outcome
T851458, T850891	1	1,030	0	Pass

All parts have passed the Pre-conditioning.

6.2. Temperature Cycling

A total of 154 devices were tested with temperature cycling. Temperature cycling stresses devices between -55°C to +125°C at 3 cycles per hour for 1,000 cycles. This test is used for analysis of package performance.

Table 2 – Temperature Cycling Results

Wafer Lot	# of Cycles	Sample Size	Devices Failed	Test Outcome
T851458	1,000	77	0	Pass
T850891	1,000	77	0	Pass

All parts have passed the Temperature Cycling test.

6.3. Unbiased HAST Test (Highly Accelerated Temperature/Humidity Stress Test)

A total 154 devices were tested for HAST. The HAST is done at +130°C and 85% relative humidity for 96 hours. This test is used for analysis of package performance.

Table 3 – Unbiased HAST Results

Wafer Lot	Test Duration (hours)	Sample Size	Devices Failed	Test Outcome
T851458	96	77	0	Pass
T850891	96	77	0	Pass

All parts have passed the unbiased HAST test.

6.4. Biased HAST Test (Biased Highly Accelerated Stress Test)

A total 1,155 devices were tested on biased HAST. The HAST is done at +130°C and 85% relative humidity under 4.0 V bias for 96 hours. This test is used for analysis of package performance under extreme operating conditions.

Table 4 – Biased HAST Results

Wafer Lot	Test Duration (hours)	Sample Size	Devices Failed	Test Outcome
T851458	96	77	0	Pass
T850891	96	77	0	Pass

All parts have passed the biased HAST test.

6.5.1 HTOL Test (High Temperature Operation Life Test)

A total of 154 devices were tested HTOL. This test is used for analysis of life time of the device under extreme operating conditions.

Table 5 – HTOL Results

Wafer Lot	Sample Size	# of Hours	Bias Condition	Devices Failed	Test Outcome
T850891	77	1,000	5.5 V @ +150°C	0	Pass
T851458	77	1,000	3.7 V @ +150°C	0	Pass

All parts have passed the HTOL test.

6.5.2 Early Life Failure Rate

Total of 150 units of various lots were stressed with high temperature life stress conditions (4.O V, +150C) for 168 hours. These units all passed the electrical test following the stress, there are no failures.

6.6. *High Temperature Storage Test*

A total of 154 devices were tested on high temperature storage. This test is used for analysis of device performance.

Table 6 – High Temperature Storage Results

Wafer Lot	Sample Size	# of Hours	Bake Temperature	Devices Failed	Test Outcome
T850891	77	1,000	@ +150°C	0	Pass
T851458	77	1,000	@ +150°C	0	Pass

All parts have passed the high temperature storage test.

6.7. *ESD (HBM)*

Human Body Model test was performed on a number of samples from one (1) lot of RR1X2 series to characterize the susceptibility of devices to damage from electrostatic discharge (ESD) induced by human handling. Resulting data did not show any notable change due to ESD. The products are qualified for ±4kV per JEDEC-JS001-2014.

6.8. *Latch-up (LU)*

The latch-up characterization was successfully completed on samples from one (1) lot of RR1X2 series using excessive current flow between the power supply and ground as well as output to power pin and to ground. The products are qualified per JESD78.

7. Conclusion

The RR12X series of products were tested as described in this report. All devices were electrically tested, and sample units were magnetically tested per the datasheet's specifications. This is an initial qualification report. Final qualification is in progress.

Revision History:

Revision	Date	Description
0.0	8/15/2019	Initial Release – Pre-qualification Report